**Team #09**

**Title: Project 5 Report**

**Course: Advanced Digital System Design (Fall 2022)**

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**REPORT**

Design Summary:

In this Project, we will integrate an IP core of our own design to the Arm Cortex-A9 processor in the Cyclone V SoC on the DE1-SoC board. We will test our IP core using a Linux kernel module. The kernel module will provide a common programmable interface to userland software. Completion of this assignment will yield a starting roadmap to multiple fields such as SoC design, and heterogeneous computing.

*Part 1*

Text

Description automatically generated

Pin assignment for DE1-Soc Board

TOP level Module code

library ieee;

use ieee.std\_logic\_1164.all;

entity toplevel is

port (

clk\_clk : in std\_logic := 'X'; -- clk

hps\_io\_hps\_io\_emac1\_inst\_TX\_CLK : out std\_logic; -- hps\_io\_emac1\_inst\_TX\_CLK

hps\_io\_hps\_io\_emac1\_inst\_TXD0 : out std\_logic; -- hps\_io\_emac1\_inst\_TXD0

hps\_io\_hps\_io\_emac1\_inst\_TXD1 : out std\_logic; -- hps\_io\_emac1\_inst\_TXD1

hps\_io\_hps\_io\_emac1\_inst\_TXD2 : out std\_logic; -- hps\_io\_emac1\_inst\_TXD2

hps\_io\_hps\_io\_emac1\_inst\_TXD3 : out std\_logic; -- hps\_io\_emac1\_inst\_TXD3

hps\_io\_hps\_io\_emac1\_inst\_RXD0 : in std\_logic := 'X'; -- hps\_io\_emac1\_inst\_RXD0

hps\_io\_hps\_io\_emac1\_inst\_MDIO : inout std\_logic := 'X'; -- hps\_io\_emac1\_inst\_MDIO

hps\_io\_hps\_io\_emac1\_inst\_MDC : out std\_logic; -- hps\_io\_emac1\_inst\_MDC

hps\_io\_hps\_io\_emac1\_inst\_RX\_CTL : in std\_logic := 'X'; -- hps\_io\_emac1\_inst\_RX\_CTL

hps\_io\_hps\_io\_emac1\_inst\_TX\_CTL : out std\_logic; -- hps\_io\_emac1\_inst\_TX\_CTL

hps\_io\_hps\_io\_emac1\_inst\_RX\_CLK : in std\_logic := 'X'; -- hps\_io\_emac1\_inst\_RX\_CLK

hps\_io\_hps\_io\_emac1\_inst\_RXD1 : in std\_logic := 'X'; -- hps\_io\_emac1\_inst\_RXD1

hps\_io\_hps\_io\_emac1\_inst\_RXD2 : in std\_logic := 'X'; -- hps\_io\_emac1\_inst\_RXD2

hps\_io\_hps\_io\_emac1\_inst\_RXD3 : in std\_logic := 'X'; -- hps\_io\_emac1\_inst\_RXD3

hps\_io\_hps\_io\_qspi\_inst\_IO0 : inout std\_logic := 'X'; -- hps\_io\_qspi\_inst\_IO0

hps\_io\_hps\_io\_qspi\_inst\_IO1 : inout std\_logic := 'X'; -- hps\_io\_qspi\_inst\_IO1

hps\_io\_hps\_io\_qspi\_inst\_IO2 : inout std\_logic := 'X'; -- hps\_io\_qspi\_inst\_IO2

hps\_io\_hps\_io\_qspi\_inst\_IO3 : inout std\_logic := 'X'; -- hps\_io\_qspi\_inst\_IO3

hps\_io\_hps\_io\_qspi\_inst\_SS0 : out std\_logic; -- hps\_io\_qspi\_inst\_SS0

hps\_io\_hps\_io\_qspi\_inst\_CLK : out std\_logic; -- hps\_io\_qspi\_inst\_CLK

hps\_io\_hps\_io\_sdio\_inst\_CMD : inout std\_logic := 'X'; -- hps\_io\_sdio\_inst\_CMD

hps\_io\_hps\_io\_sdio\_inst\_D0 : inout std\_logic := 'X'; -- hps\_io\_sdio\_inst\_D0

hps\_io\_hps\_io\_sdio\_inst\_D1 : inout std\_logic := 'X'; -- hps\_io\_sdio\_inst\_D1

hps\_io\_hps\_io\_sdio\_inst\_CLK : out std\_logic; -- hps\_io\_sdio\_inst\_CLK

hps\_io\_hps\_io\_sdio\_inst\_D2 : inout std\_logic := 'X'; -- hps\_io\_sdio\_inst\_D2

hps\_io\_hps\_io\_sdio\_inst\_D3 : inout std\_logic := 'X'; -- hps\_io\_sdio\_inst\_D3

hps\_io\_hps\_io\_usb1\_inst\_D0 : inout std\_logic := 'X'; -- hps\_io\_usb1\_inst\_D0

hps\_io\_hps\_io\_usb1\_inst\_D1 : inout std\_logic := 'X'; -- hps\_io\_usb1\_inst\_D1

hps\_io\_hps\_io\_usb1\_inst\_D2 : inout std\_logic := 'X'; -- hps\_io\_usb1\_inst\_D2

hps\_io\_hps\_io\_usb1\_inst\_D3 : inout std\_logic := 'X'; -- hps\_io\_usb1\_inst\_D3

hps\_io\_hps\_io\_usb1\_inst\_D4 : inout std\_logic := 'X'; -- hps\_io\_usb1\_inst\_D4

hps\_io\_hps\_io\_usb1\_inst\_D5 : inout std\_logic := 'X'; -- hps\_io\_usb1\_inst\_D5

hps\_io\_hps\_io\_usb1\_inst\_D6 : inout std\_logic := 'X'; -- hps\_io\_usb1\_inst\_D6

hps\_io\_hps\_io\_usb1\_inst\_D7 : inout std\_logic := 'X'; -- hps\_io\_usb1\_inst\_D7

hps\_io\_hps\_io\_usb1\_inst\_CLK : in std\_logic := 'X'; -- hps\_io\_usb1\_inst\_CLK

hps\_io\_hps\_io\_usb1\_inst\_STP : out std\_logic; -- hps\_io\_usb1\_inst\_STP

hps\_io\_hps\_io\_usb1\_inst\_DIR : in std\_logic := 'X'; -- hps\_io\_usb1\_inst\_DIR

hps\_io\_hps\_io\_usb1\_inst\_NXT : in std\_logic := 'X'; -- hps\_io\_usb1\_inst\_NXT

hps\_io\_hps\_io\_spim1\_inst\_CLK : out std\_logic; -- hps\_io\_spim1\_inst\_CLK

hps\_io\_hps\_io\_spim1\_inst\_MOSI : out std\_logic; -- hps\_io\_spim1\_inst\_MOSI

hps\_io\_hps\_io\_spim1\_inst\_MISO : in std\_logic := 'X'; -- hps\_io\_spim1\_inst\_MISO

hps\_io\_hps\_io\_spim1\_inst\_SS0 : out std\_logic; -- hps\_io\_spim1\_inst\_SS0

hps\_io\_hps\_io\_uart0\_inst\_RX : in std\_logic := 'X'; -- hps\_io\_uart0\_inst\_RX

hps\_io\_hps\_io\_uart0\_inst\_TX : out std\_logic; -- hps\_io\_uart0\_inst\_TX

hps\_io\_hps\_io\_i2c0\_inst\_SDA : inout std\_logic := 'X'; -- hps\_io\_i2c0\_inst\_SDA

hps\_io\_hps\_io\_i2c0\_inst\_SCL : inout std\_logic := 'X'; -- hps\_io\_i2c0\_inst\_SCL

hps\_io\_hps\_io\_i2c1\_inst\_SDA : inout std\_logic := 'X'; -- hps\_io\_i2c1\_inst\_SDA

hps\_io\_hps\_io\_i2c1\_inst\_SCL : inout std\_logic := 'X'; -- hps\_io\_i2c1\_inst\_SCL

memory\_mem\_a : out std\_logic\_vector(14 downto 0); -- mem\_a

memory\_mem\_ba : out std\_logic\_vector(2 downto 0); -- mem\_ba

memory\_mem\_ck : out std\_logic; -- mem\_ck

memory\_mem\_ck\_n : out std\_logic; -- mem\_ck\_n

memory\_mem\_cke : out std\_logic; -- mem\_cke

memory\_mem\_cs\_n : out std\_logic; -- mem\_cs\_n

memory\_mem\_ras\_n : out std\_logic; -- mem\_ras\_n

memory\_mem\_cas\_n : out std\_logic; -- mem\_cas\_n

memory\_mem\_we\_n : out std\_logic; -- mem\_we\_n

memory\_mem\_reset\_n : out std\_logic; -- mem\_reset\_n

memory\_mem\_dq : inout std\_logic\_vector(31 downto 0) := (others => 'X'); -- mem\_dq

memory\_mem\_dqs : inout std\_logic\_vector(3 downto 0) := (others => 'X'); -- mem\_dqs

memory\_mem\_dqs\_n : inout std\_logic\_vector(3 downto 0) := (others => 'X'); -- mem\_dqs\_n

memory\_mem\_odt : out std\_logic; -- mem\_odt

memory\_mem\_dm : out std\_logic\_vector(3 downto 0); -- mem\_dm

memory\_oct\_rzqin : in std\_logic := 'X'; -- oct\_rzqin

digits : out std\_logic\_vector(41 downto 0) -- export

);

end entity toplevel;

architecture rtl of toplevel is

component soc\_calc\_base is

port (

clk\_clk : in std\_logic := 'X'; -- clk

hps\_io\_hps\_io\_emac1\_inst\_TX\_CLK : out std\_logic; -- hps\_io\_emac1\_inst\_TX\_CLK

hps\_io\_hps\_io\_emac1\_inst\_TXD0 : out std\_logic; -- hps\_io\_emac1\_inst\_TXD0

hps\_io\_hps\_io\_emac1\_inst\_TXD1 : out std\_logic; -- hps\_io\_emac1\_inst\_TXD1

hps\_io\_hps\_io\_emac1\_inst\_TXD2 : out std\_logic; -- hps\_io\_emac1\_inst\_TXD2

hps\_io\_hps\_io\_emac1\_inst\_TXD3 : out std\_logic; -- hps\_io\_emac1\_inst\_TXD3

hps\_io\_hps\_io\_emac1\_inst\_RXD0 : in std\_logic := 'X'; -- hps\_io\_emac1\_inst\_RXD0

hps\_io\_hps\_io\_emac1\_inst\_MDIO : inout std\_logic := 'X'; -- hps\_io\_emac1\_inst\_MDIO

hps\_io\_hps\_io\_emac1\_inst\_MDC : out std\_logic; -- hps\_io\_emac1\_inst\_MDC

hps\_io\_hps\_io\_emac1\_inst\_RX\_CTL : in std\_logic := 'X'; -- hps\_io\_emac1\_inst\_RX\_CTL

hps\_io\_hps\_io\_emac1\_inst\_TX\_CTL : out std\_logic; -- hps\_io\_emac1\_inst\_TX\_CTL

hps\_io\_hps\_io\_emac1\_inst\_RX\_CLK : in std\_logic := 'X'; -- hps\_io\_emac1\_inst\_RX\_CLK

hps\_io\_hps\_io\_emac1\_inst\_RXD1 : in std\_logic := 'X'; -- hps\_io\_emac1\_inst\_RXD1

hps\_io\_hps\_io\_emac1\_inst\_RXD2 : in std\_logic := 'X'; -- hps\_io\_emac1\_inst\_RXD2

hps\_io\_hps\_io\_emac1\_inst\_RXD3 : in std\_logic := 'X'; -- hps\_io\_emac1\_inst\_RXD3

hps\_io\_hps\_io\_qspi\_inst\_IO0 : inout std\_logic := 'X'; -- hps\_io\_qspi\_inst\_IO0

hps\_io\_hps\_io\_qspi\_inst\_IO1 : inout std\_logic := 'X'; -- hps\_io\_qspi\_inst\_IO1

hps\_io\_hps\_io\_qspi\_inst\_IO2 : inout std\_logic := 'X'; -- hps\_io\_qspi\_inst\_IO2

hps\_io\_hps\_io\_qspi\_inst\_IO3 : inout std\_logic := 'X'; -- hps\_io\_qspi\_inst\_IO3

hps\_io\_hps\_io\_qspi\_inst\_SS0 : out std\_logic; -- hps\_io\_qspi\_inst\_SS0

hps\_io\_hps\_io\_qspi\_inst\_CLK : out std\_logic; -- hps\_io\_qspi\_inst\_CLK

hps\_io\_hps\_io\_sdio\_inst\_CMD : inout std\_logic := 'X'; -- hps\_io\_sdio\_inst\_CMD

hps\_io\_hps\_io\_sdio\_inst\_D0 : inout std\_logic := 'X'; -- hps\_io\_sdio\_inst\_D0

hps\_io\_hps\_io\_sdio\_inst\_D1 : inout std\_logic := 'X'; -- hps\_io\_sdio\_inst\_D1

hps\_io\_hps\_io\_sdio\_inst\_CLK : out std\_logic; -- hps\_io\_sdio\_inst\_CLK

hps\_io\_hps\_io\_sdio\_inst\_D2 : inout std\_logic := 'X'; -- hps\_io\_sdio\_inst\_D2

hps\_io\_hps\_io\_sdio\_inst\_D3 : inout std\_logic := 'X'; -- hps\_io\_sdio\_inst\_D3

hps\_io\_hps\_io\_usb1\_inst\_D0 : inout std\_logic := 'X'; -- hps\_io\_usb1\_inst\_D0

hps\_io\_hps\_io\_usb1\_inst\_D1 : inout std\_logic := 'X'; -- hps\_io\_usb1\_inst\_D1

hps\_io\_hps\_io\_usb1\_inst\_D2 : inout std\_logic := 'X'; -- hps\_io\_usb1\_inst\_D2

hps\_io\_hps\_io\_usb1\_inst\_D3 : inout std\_logic := 'X'; -- hps\_io\_usb1\_inst\_D3

hps\_io\_hps\_io\_usb1\_inst\_D4 : inout std\_logic := 'X'; -- hps\_io\_usb1\_inst\_D4

hps\_io\_hps\_io\_usb1\_inst\_D5 : inout std\_logic := 'X'; -- hps\_io\_usb1\_inst\_D5

hps\_io\_hps\_io\_usb1\_inst\_D6 : inout std\_logic := 'X'; -- hps\_io\_usb1\_inst\_D6

hps\_io\_hps\_io\_usb1\_inst\_D7 : inout std\_logic := 'X'; -- hps\_io\_usb1\_inst\_D7

hps\_io\_hps\_io\_usb1\_inst\_CLK : in std\_logic := 'X'; -- hps\_io\_usb1\_inst\_CLK

hps\_io\_hps\_io\_usb1\_inst\_STP : out std\_logic; -- hps\_io\_usb1\_inst\_STP

hps\_io\_hps\_io\_usb1\_inst\_DIR : in std\_logic := 'X'; -- hps\_io\_usb1\_inst\_DIR

hps\_io\_hps\_io\_usb1\_inst\_NXT : in std\_logic := 'X'; -- hps\_io\_usb1\_inst\_NXT

hps\_io\_hps\_io\_spim1\_inst\_CLK : out std\_logic; -- hps\_io\_spim1\_inst\_CLK

hps\_io\_hps\_io\_spim1\_inst\_MOSI : out std\_logic; -- hps\_io\_spim1\_inst\_MOSI

hps\_io\_hps\_io\_spim1\_inst\_MISO : in std\_logic := 'X'; -- hps\_io\_spim1\_inst\_MISO

hps\_io\_hps\_io\_spim1\_inst\_SS0 : out std\_logic; -- hps\_io\_spim1\_inst\_SS0

hps\_io\_hps\_io\_uart0\_inst\_RX : in std\_logic := 'X'; -- hps\_io\_uart0\_inst\_RX

hps\_io\_hps\_io\_uart0\_inst\_TX : out std\_logic; -- hps\_io\_uart0\_inst\_TX

hps\_io\_hps\_io\_i2c0\_inst\_SDA : inout std\_logic := 'X'; -- hps\_io\_i2c0\_inst\_SDA

hps\_io\_hps\_io\_i2c0\_inst\_SCL : inout std\_logic := 'X'; -- hps\_io\_i2c0\_inst\_SCL

hps\_io\_hps\_io\_i2c1\_inst\_SDA : inout std\_logic := 'X'; -- hps\_io\_i2c1\_inst\_SDA

hps\_io\_hps\_io\_i2c1\_inst\_SCL : inout std\_logic := 'X'; -- hps\_io\_i2c1\_inst\_SCL

memory\_mem\_a : out std\_logic\_vector(14 downto 0); -- mem\_a

memory\_mem\_ba : out std\_logic\_vector(2 downto 0); -- mem\_ba

memory\_mem\_ck : out std\_logic; -- mem\_ck

memory\_mem\_ck\_n : out std\_logic; -- mem\_ck\_n

memory\_mem\_cke : out std\_logic; -- mem\_cke

memory\_mem\_cs\_n : out std\_logic; -- mem\_cs\_n

memory\_mem\_ras\_n : out std\_logic; -- mem\_ras\_n

memory\_mem\_cas\_n : out std\_logic; -- mem\_cas\_n

memory\_mem\_we\_n : out std\_logic; -- mem\_we\_n

memory\_mem\_reset\_n : out std\_logic; -- mem\_reset\_n

memory\_mem\_dq : inout std\_logic\_vector(31 downto 0) := (others => 'X'); -- mem\_dq

memory\_mem\_dqs : inout std\_logic\_vector(3 downto 0) := (others => 'X'); -- mem\_dqs

memory\_mem\_dqs\_n : inout std\_logic\_vector(3 downto 0) := (others => 'X'); -- mem\_dqs\_n

memory\_mem\_odt : out std\_logic; -- mem\_odt

memory\_mem\_dm : out std\_logic\_vector(3 downto 0); -- mem\_dm

memory\_oct\_rzqin : in std\_logic := 'X'; -- oct\_rzqin

reset\_reset\_n : in std\_logic := 'X'; -- reset\_n

digits\_export : out std\_logic\_vector(41 downto 0) -- export

);

end component soc\_calc\_base;

begin

u0 : component soc\_calc\_base

port map (

clk\_clk => clk\_clk, -- clk.clk

hps\_io\_hps\_io\_emac1\_inst\_TX\_CLK => hps\_io\_hps\_io\_emac1\_inst\_TX\_CLK, -- hps\_io.hps\_io\_emac1\_inst\_TX\_CLK

hps\_io\_hps\_io\_emac1\_inst\_TXD0 => hps\_io\_hps\_io\_emac1\_inst\_TXD0, -- .hps\_io\_emac1\_inst\_TXD0

hps\_io\_hps\_io\_emac1\_inst\_TXD1 => hps\_io\_hps\_io\_emac1\_inst\_TXD1, -- .hps\_io\_emac1\_inst\_TXD1

hps\_io\_hps\_io\_emac1\_inst\_TXD2 => hps\_io\_hps\_io\_emac1\_inst\_TXD2, -- .hps\_io\_emac1\_inst\_TXD2

hps\_io\_hps\_io\_emac1\_inst\_TXD3 => hps\_io\_hps\_io\_emac1\_inst\_TXD3, -- .hps\_io\_emac1\_inst\_TXD3

hps\_io\_hps\_io\_emac1\_inst\_RXD0 => hps\_io\_hps\_io\_emac1\_inst\_RXD0, -- .hps\_io\_emac1\_inst\_RXD0

hps\_io\_hps\_io\_emac1\_inst\_MDIO => hps\_io\_hps\_io\_emac1\_inst\_MDIO, -- .hps\_io\_emac1\_inst\_MDIO

hps\_io\_hps\_io\_emac1\_inst\_MDC => hps\_io\_hps\_io\_emac1\_inst\_MDC, -- .hps\_io\_emac1\_inst\_MDC

hps\_io\_hps\_io\_emac1\_inst\_RX\_CTL => hps\_io\_hps\_io\_emac1\_inst\_RX\_CTL, -- .hps\_io\_emac1\_inst\_RX\_CTL

hps\_io\_hps\_io\_emac1\_inst\_TX\_CTL => hps\_io\_hps\_io\_emac1\_inst\_TX\_CTL, -- .hps\_io\_emac1\_inst\_TX\_CTL

hps\_io\_hps\_io\_emac1\_inst\_RX\_CLK => hps\_io\_hps\_io\_emac1\_inst\_RX\_CLK, -- .hps\_io\_emac1\_inst\_RX\_CLK

hps\_io\_hps\_io\_emac1\_inst\_RXD1 => hps\_io\_hps\_io\_emac1\_inst\_RXD1, -- .hps\_io\_emac1\_inst\_RXD1

hps\_io\_hps\_io\_emac1\_inst\_RXD2 => hps\_io\_hps\_io\_emac1\_inst\_RXD2, -- .hps\_io\_emac1\_inst\_RXD2

hps\_io\_hps\_io\_emac1\_inst\_RXD3 => hps\_io\_hps\_io\_emac1\_inst\_RXD3, -- .hps\_io\_emac1\_inst\_RXD3

hps\_io\_hps\_io\_qspi\_inst\_IO0 => hps\_io\_hps\_io\_qspi\_inst\_IO0, -- .hps\_io\_qspi\_inst\_IO0

hps\_io\_hps\_io\_qspi\_inst\_IO1 => hps\_io\_hps\_io\_qspi\_inst\_IO1, -- .hps\_io\_qspi\_inst\_IO1

hps\_io\_hps\_io\_qspi\_inst\_IO2 => hps\_io\_hps\_io\_qspi\_inst\_IO2, -- .hps\_io\_qspi\_inst\_IO2

hps\_io\_hps\_io\_qspi\_inst\_IO3 => hps\_io\_hps\_io\_qspi\_inst\_IO3, -- .hps\_io\_qspi\_inst\_IO3

hps\_io\_hps\_io\_qspi\_inst\_SS0 => hps\_io\_hps\_io\_qspi\_inst\_SS0, -- .hps\_io\_qspi\_inst\_SS0

hps\_io\_hps\_io\_qspi\_inst\_CLK => hps\_io\_hps\_io\_qspi\_inst\_CLK, -- .hps\_io\_qspi\_inst\_CLK

hps\_io\_hps\_io\_sdio\_inst\_CMD => hps\_io\_hps\_io\_sdio\_inst\_CMD, -- .hps\_io\_sdio\_inst\_CMD

hps\_io\_hps\_io\_sdio\_inst\_D0 => hps\_io\_hps\_io\_sdio\_inst\_D0, -- .hps\_io\_sdio\_inst\_D0

hps\_io\_hps\_io\_sdio\_inst\_D1 => hps\_io\_hps\_io\_sdio\_inst\_D1, -- .hps\_io\_sdio\_inst\_D1

hps\_io\_hps\_io\_sdio\_inst\_CLK => hps\_io\_hps\_io\_sdio\_inst\_CLK, -- .hps\_io\_sdio\_inst\_CLK

hps\_io\_hps\_io\_sdio\_inst\_D2 => hps\_io\_hps\_io\_sdio\_inst\_D2, -- .hps\_io\_sdio\_inst\_D2

hps\_io\_hps\_io\_sdio\_inst\_D3 => hps\_io\_hps\_io\_sdio\_inst\_D3, -- .hps\_io\_sdio\_inst\_D3

hps\_io\_hps\_io\_usb1\_inst\_D0 => hps\_io\_hps\_io\_usb1\_inst\_D0, -- .hps\_io\_usb1\_inst\_D0

hps\_io\_hps\_io\_usb1\_inst\_D1 => hps\_io\_hps\_io\_usb1\_inst\_D1, -- .hps\_io\_usb1\_inst\_D1

hps\_io\_hps\_io\_usb1\_inst\_D2 => hps\_io\_hps\_io\_usb1\_inst\_D2, -- .hps\_io\_usb1\_inst\_D2

hps\_io\_hps\_io\_usb1\_inst\_D3 => hps\_io\_hps\_io\_usb1\_inst\_D3, -- .hps\_io\_usb1\_inst\_D3

hps\_io\_hps\_io\_usb1\_inst\_D4 => hps\_io\_hps\_io\_usb1\_inst\_D4, -- .hps\_io\_usb1\_inst\_D4

hps\_io\_hps\_io\_usb1\_inst\_D5 => hps\_io\_hps\_io\_usb1\_inst\_D5, -- .hps\_io\_usb1\_inst\_D5

hps\_io\_hps\_io\_usb1\_inst\_D6 => hps\_io\_hps\_io\_usb1\_inst\_D6, -- .hps\_io\_usb1\_inst\_D6

hps\_io\_hps\_io\_usb1\_inst\_D7 => hps\_io\_hps\_io\_usb1\_inst\_D7, -- .hps\_io\_usb1\_inst\_D7

hps\_io\_hps\_io\_usb1\_inst\_CLK => hps\_io\_hps\_io\_usb1\_inst\_CLK, -- .hps\_io\_usb1\_inst\_CLK

hps\_io\_hps\_io\_usb1\_inst\_STP => hps\_io\_hps\_io\_usb1\_inst\_STP, -- .hps\_io\_usb1\_inst\_STP

hps\_io\_hps\_io\_usb1\_inst\_DIR => hps\_io\_hps\_io\_usb1\_inst\_DIR, -- .hps\_io\_usb1\_inst\_DIR

hps\_io\_hps\_io\_usb1\_inst\_NXT => hps\_io\_hps\_io\_usb1\_inst\_NXT, -- .hps\_io\_usb1\_inst\_NXT

hps\_io\_hps\_io\_spim1\_inst\_CLK => hps\_io\_hps\_io\_spim1\_inst\_CLK, -- .hps\_io\_spim1\_inst\_CLK

hps\_io\_hps\_io\_spim1\_inst\_MOSI => hps\_io\_hps\_io\_spim1\_inst\_MOSI, -- .hps\_io\_spim1\_inst\_MOSI

hps\_io\_hps\_io\_spim1\_inst\_MISO => hps\_io\_hps\_io\_spim1\_inst\_MISO, -- .hps\_io\_spim1\_inst\_MISO

hps\_io\_hps\_io\_spim1\_inst\_SS0 => hps\_io\_hps\_io\_spim1\_inst\_SS0, -- .hps\_io\_spim1\_inst\_SS0

hps\_io\_hps\_io\_uart0\_inst\_RX => hps\_io\_hps\_io\_uart0\_inst\_RX, -- .hps\_io\_uart0\_inst\_RX

hps\_io\_hps\_io\_uart0\_inst\_TX => hps\_io\_hps\_io\_uart0\_inst\_TX, -- .hps\_io\_uart0\_inst\_TX

hps\_io\_hps\_io\_i2c0\_inst\_SDA => hps\_io\_hps\_io\_i2c0\_inst\_SDA, -- .hps\_io\_i2c0\_inst\_SDA

hps\_io\_hps\_io\_i2c0\_inst\_SCL => hps\_io\_hps\_io\_i2c0\_inst\_SCL, -- .hps\_io\_i2c0\_inst\_SCL

hps\_io\_hps\_io\_i2c1\_inst\_SDA => hps\_io\_hps\_io\_i2c1\_inst\_SDA, -- .hps\_io\_i2c1\_inst\_SDA

hps\_io\_hps\_io\_i2c1\_inst\_SCL => hps\_io\_hps\_io\_i2c1\_inst\_SCL, -- .hps\_io\_i2c1\_inst\_SCL

memory\_mem\_a => memory\_mem\_a, -- memory.mem\_a

memory\_mem\_ba => memory\_mem\_ba, -- .mem\_ba

memory\_mem\_ck => memory\_mem\_ck, -- .mem\_ck

memory\_mem\_ck\_n => memory\_mem\_ck\_n, -- .mem\_ck\_n

memory\_mem\_cke => memory\_mem\_cke, -- .mem\_cke

memory\_mem\_cs\_n => memory\_mem\_cs\_n, -- .mem\_cs\_n

memory\_mem\_ras\_n => memory\_mem\_ras\_n, -- .mem\_ras\_n

memory\_mem\_cas\_n => memory\_mem\_cas\_n, -- .mem\_cas\_n

memory\_mem\_we\_n => memory\_mem\_we\_n, -- .mem\_we\_n

memory\_mem\_reset\_n => memory\_mem\_reset\_n, -- .mem\_reset\_n

memory\_mem\_dq => memory\_mem\_dq, -- .mem\_dq

memory\_mem\_dqs => memory\_mem\_dqs, -- .mem\_dqs

memory\_mem\_dqs\_n => memory\_mem\_dqs\_n, -- .mem\_dqs\_n

memory\_mem\_odt => memory\_mem\_odt, -- .mem\_odt

memory\_mem\_dm => memory\_mem\_dm, -- .mem\_dm

memory\_oct\_rzqin => memory\_oct\_rzqin, -- .oct\_rzqin

reset\_reset\_n => '1', -- reset.reset\_n

digits\_export => digits -- digits.export

);

end architecture rtl;

Simulation

Text

Description automatically generated

Text

Description automatically generated

Text

Description automatically generated with medium confidence

Shell Output

A picture containing indoor, light

Description automatically generated

Output on the Board

Text

Description automatically generated